AMENDMENTS TO THE CLAIMS

Please amend claims 32, 40, 50 and 51 as follows:

1-31. (Previously Canceled)

32. (Currently Amended) An integrated circuit comprising:

a reflective layer having a reflective surface;

a first anti-reflective coating over the reflective surface, the first coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface;

a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction and the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

33. (Canceled)

34. (Original) The integrated circuit according to claim 32, wherein the second antireflective coating is on the entire upper surface of said first anti-reflective coating.

35. (Original) The integrated circuit according to claim 32, wherein the material placed over the second coating is photoresist placed in contact with the second coating during the manufacturing process.

36. (Original) The integrated circuit according to claim 32, further comprising at least one additional anti-reflective coating over the first and second coatings.

37. (Original) The integrated circuit according to claim 32, further comprising a dielectric material between the photoresist and the second coating.

38. (Original) The integrated circuit according to claim 32, wherein the thickness of the first coating is approximately 40 nanometers and the thickness of the second coating is approximately 25 nanometers.

B1 cont.

39. (Original) The integrated circuit according to claim 32, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

40. (Currently Amended) A memory cell comprising:

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface and adapted to stop an etch process;

a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface and adapted to stop an etch process; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

B, cont.

41. (Original) The integrated circuit according to claim 40, wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

42. (Original) The memory cell according to claim 40, wherein the second anti-reflective coating is formed entirely on said first anti-reflective coating.

43. (Original) The memory cell according to claim 40, wherein the first and second coatings are below the insulating layer.

44. (Original) The memory cell according to claim 40, wherein the structure is a dual DRAM cell structure comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line.

45. (Original) The memory cell according to claim 44, wherein the capacitors are formed over the gate stacks.

B1 cont.

46. (Original) The memory cell according to claim 45, wherein the capacitors are container capacitors.

47. (Original) The memory cell according to claim 44, wherein the bit line is formed over the capacitors.

48. (Original) The memory cell according to claim 40, wherein the thickness of the first layer is approximately 40 nanometers and the thickness of the second layer is approximately 25 nanometers.

49. (Original) The integrated circuit according to claim 40, where the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

50. (Currently Amended) An integrated circuit comprising:

at least one memory cell, the memory cell comprising

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; ~~and~~

a capacitor in electrical contact with one of the active areas;

an etch stop layer comprising:

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption;

a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

51. (Currently Amended) A computer system comprising:

a processor; and

a memory, the memory comprising at least one memory cell, the memory cell comprising

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption and adapted to stop an etch process;

a second anti-reflective coating formed on the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption and adapted to stop an etch process; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

B1 cont.

52. (Previously Canceled)

53. (Previously Canceled)

54. (Previously Canceled)

55. (Withdrawn)

56. (Withdrawn)

57. (Withdrawn)

58. (New) The integrated circuit according to claim 32, wherein the inter-level dielectric layer is located between said first and second anti-reflective coatings.

59. (New) The integrated circuit according to claim 32, wherein the inter-level dielectric layer is located below said first and second anti-reflective coatings.

60. (New) An integrated circuit comprising:

a reflective layer having a reflective surface;

a first silicon dioxide layer over the reflective layer;

a first anti-reflective coating over the first silicon dioxide layer, the first coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface wherein the first reflective coating is on the first silicon dioxide layer;

a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction; and

a second silicon dioxide layer over the second anti-reflective coating.

61. (New) An integrated circuit comprising:

a reflective layer having a reflective surface; and

an etch layer comprising:

a first anti-reflective coating over the reflective surface, the first coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface; and

a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction.

62. (New) An integrated circuit comprising:

B2 cont.

a reflective layer having a reflective surface;

a first anti-reflective coating over the reflective surface, the first coating having properties defining a first interface;

a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having properties defining a second interface, wherein the properties of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.